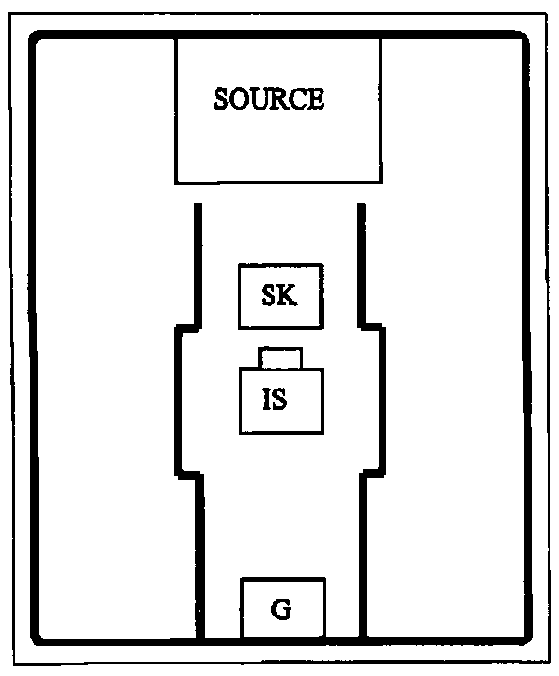
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**SK = SOURCE KELVIN**

**IS = CURRENT SENSE**

**G = GATE**



**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .035” X .047” G = .019” X .022”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .129” X .177” DATE: 9/8/21**

**MFG: IR THICKNESS .015” P/N: IRCC034**

**DG 10.1.2**

#### Rev B, 7/19/02